What Is Claimed Is:

1. A method for processing a first instruction form and a second instruction form of an instruction set in a processor comprising the steps of:

storing a plurality of instructions of the second form in a plurality of buffers proximate to a plurality of execution units;

executing at least one instruction of the first instruction form in response to a first counter; and

executing at least one instruction of the second instruction form in response to at least a second counter, wherein the second counter is invoked by a branch instruction of the first instruction form.

2. The method of claim 1, wherein the instructions of the first form and instructions of the second form are generated by a compiler based on execution frequency.

3. The method of claim 2, wherein instructions of the second form are more frequently executed than instructions of the first form.

4. The method of claim 1, wherein the step of executing at least one instruction of the second instruction form further comprises the steps of:

de-gating a plurality of execution queues storing a plurality of instructions of the first instruction form; and

pausing a fetching of the first instruction form from a memory.

5. The method of claim 1, wherein the step of executing at least one instruction of the second instruction form further comprises the steps of:

fetching at least one instruction in the buffers; and

sequencing a plurality of control signals to the execution units.

6. The method of claim 1, wherein the second instruction form is a logical subset of the first instruction form.

7. The method of claim 1, wherein the step of executing at least one instruction of the first instruction form further comprises the steps of:

fetching an instruction of the first form from a memory;

decoding the instruction; and

issuing the decoded instruction at least one execution unit.

8. The method of claim 1, wherein a return to fetching of the first instruction form is signaled by a switch bit in a buffer of a branch unit storing instructions of the second form.

9. The method of claim 1, wherein a return to fetching of the first instruction form is signaled by a return instruction of the second instruction form stored in a buffer of a branch unit.

10. The method of claim 1, wherein each execution unit is associated with one buffer.

11. A processor for processing a first instruction form and a second instruction form of an instruction set comprising:

a plurality of execution units for receiving instructions;

a branch unit connected to an instruction fetch unit for the first instruction form and a sequencer for the second instruction form;

a decode unit for decoding instructions of the first instruction form into control signals for the execution units; and

a plurality of buffers, proximate to the execution units, for storing predecoded instructions of the second instruction form.

12. The processor of claim 11, further comprising a compiler for generating the instructions of the first form and instructions of the second form based on execution frequency, wherein instructions of the second form are executed more frequently than instructions of the first form.

13. The processor of claim 11, wherein the sequencer, engaged by the branch unit, addresses the decoded instructions of the second instruction form stored in the buffers and sequences predecoded instructions of the second instruction form to the execution unit.

14. The processor of claim 11, wherein the sequencer is connected to a plurality of gates connected between a plurality of execution queues for storing the decoded instructions of the first instruction form and the plurality of execution units, the sequencer for controlling the gates.

15. The processor of claim 11, wherein each execution unit is connected to a buffer.

16. The processor of claim 11, wherein the branch unit switches the processor from the first instruction form to the second instruction form in response to a branch instruction of the first instruction form.

17. The processor of claim 11, wherein the branch unit switches the processor from the second instruction form to the first instruction form in response to a branch instruction of the second instruction form.

18. The processor of claim 11, wherein a switch bit in a buffer connected to the branch unit signals the sequencer to stop fetching from the buffers and enables instruction fetching from a memory storing instructions of the first instruction form.

19. The processor of claim 11, wherein the execution bandwidth of the execution units is larger than the fetch/issue bandwidth of the first form.

20. The processor of claim 11, wherein the second instruction form is a logical subset of the first instruction form.

21. A processor for processing a first instruction form and a second instruction form of an instruction set comprising:

a plurality of execution units for receiving instructions;

a branch unit connected to an instruction fetch unit for the first instruction form and a sequencer for the second instruction form, wherein the branch unit switches the processor from the first instruction form to the second instruction form in response to a branch instruction of the first instruction form and switches the processor from the second instruction form to the first instruction form in response to a branch instruction of the second instruction form;

a decode unit adapted to decode instructions of the first instruction form into instructions for the execution units;

an issue unit adapted to sequence decoded instructions of the first instruction form;

a plurality of buffers, proximate to the execution units, adapted to storing predecoded instructions of the second instruction form, wherein each execution unit is connected to a buffer;

a compiler adapted for generating instructions of the first form and instructions of the second form based on execution frequency, wherein instructions of the second form are executed more frequently than instructions of the first form; and

the sequencer, engaged by the branch unit, adapted to fetch the predecoded instructions and sequence the predecoded instruction of the second instruction form, wherein the sequencer is connected to a plurality of gates connected between a plurality of execution queues adapted to store the decoded instructions of the first instruction form and the plurality of execution units, the sequencer further adapted to control the gates.